What is claimed is:

1. A feedback control I/O buffer driven by a system voltage, comprising:

an input/output circuit comprising a first PMOS transistor and a first NMOS transistor and having a transmission terminal coupled to an I/O pad, wherein the first PMOS transistor has an N-well region, a gate of the first NMOS transistor receives a first gate control signal, and a drain of the first PMOS transistor serves as the transmission terminal;

a P-gate control circuit conveying a second gate control signal to the gate of the first PMOS transistor;

a feedback detection device having an input coupled to the transmission terminal to output a feedback signal according to an input voltage at the I/O pad; and

a N-well control circuit coupled to the P-gate control circuit to control the voltage level at the N-well region of the first PMOS transistor according to the feedback signal output from the feedback detection device.

2. The feedback control I/O buffer as claimed in Claim 1, wherein the N-well control circuit adjusts the voltage level at the N-well region of the first PMOS transistor to the voltage level of the input voltage when the input voltage exceeds the system voltage.

3. The feedback control I/O buffer as claimed in Claim 2, wherein the N-well control circuit adjusts the voltage level at the N-well region of the first PMOS transistor to the system voltage when the input voltage is lower than the system voltage.

4. The feedback control I/O buffer as claimed in Claim 1, wherein the input/output circuit further comprises a second NMOS transistor having a source and drain coupled to the I/O pad and the drain of the first NMOS transistor respectively, and a gate coupled to the system voltage.

5. The feedback control I/O buffer as claimed in Claim 4, wherein the N-well control circuit comprises:

a second PMOS transistor having a source coupled to the I/O pad, a gate coupled to the system voltage, and a drain coupled to the N-well region of the first PMOS transistor;

a third PMOS transistor having a gate coupled to the system voltage, a source coupled to the I/O pad, and a drain;

a fourth PMOS transistor having a gate coupled to the drain of the third PMOS transistor, a drain coupled to the system voltage, and a source coupled to the N-well region of the first PMOS transistor;

a third NMOS transistor having a gate coupled to the feedback signal from the feedback detection device, and a source coupled to the ground; and

a fourth NMOS transistor having a gate coupled to the system voltage, a source coupled to a drain of the

third NMOS transistor, and a drain coupled to the gate of the fourth transistor.

6. The feedback control I/O buffer as claimed in Claim 5, wherein the P-gate control circuit comprises:

a transmission gate having a fifth NMOS transistor and a fifth PMOS transistor, the sources of which are coupled to the second gate control signal, the drains of which are coupled to the gate of the first PMOS transistor, and the gates of which are coupled to the system voltage and a drain of the third PMOS transistor respectively; and

a sixth PMOS transistor having a gate coupled to the system voltage, a drain coupled to the gate of the first PMOS transistor, and a source coupled to the source of the fourth transistor and the N-well region of the first PMOS transistor.

7. The feedback control I/O buffer as claimed in Claim 1, wherein the feedback detection device is an inverter.

8. The feedback control I/O buffer as claimed in Claim 7, wherein the inverter comprises:

a sixth NMOS transistor having a source coupled to the ground and a drain coupled to the gate of the third NMOS transistor;

a seventh PMOS transistor having a source coupled to the system voltage and a drain coupled to the drain of the sixth NMOS transistor; and

a seventh NMOS transistor having a gate coupled to the system voltage, a drain coupled to the I/O pad, and

a source coupled to gates of the sixth NMOS transistor and the seventh PMOS transistor.

9. An input/output buffer, comprising:

a floating N-well;

a first NMOS transistor having a gate coupled to a first gate control signal, a source coupled to the ground;

a second NMOS transistor having a gate coupled to a system voltage, a source coupled to a drain of the first NMOS transistor and a drain coupled to an I/O pad;

an inverter having an input terminal coupled to the I/O pad, and an output terminal;

a third NMOS transistor having a gate coupled to the output terminal of the inverter and a source coupled to the ground;

a fourth NMOS transistor having a source coupled to the drain of the third NMOS transistor, and a gate coupled to the system voltage;

a first PMOS transistor having a source coupled to the system voltage, and a drain coupled to the I/O pad;

a second PMOS transistor having a source coupled to the I/O pad, a gate coupled to the system voltage, and a drain coupled to the floating N-well;

a third PMOS transistor having a source coupled to I/O pad, a gate coupled to the system voltage, and a drain coupled to a source of the fourth NMOS transistor;

a fourth PMOS transistor having a gate coupled the drain of the third PMOS transistor, a drain coupled to

the system voltage, and a source coupled to the floating N-well;

a transmission gate including a fifth NMOS transistor and a fifth PMOS transistor, the sources of which are coupled to a second gate control signal, the drains of which are coupled to the gate of the first PMOS transistor, and the gates of which are coupled to a drain of the third PMOS transistor and the system voltage respectively;

a sixth PMOS transistor having a gate coupled to the system voltage, a drain coupled to the gate of the first PMOS transistor and a source coupled to the floating N-well and the source of the fourth PMOS transistor; wherein the floating N-well is connected to the substrate on which the first to sixth PMOS transistors are formed.

10. The input/output buffer as claimed in claim 9, wherein the inverter comprises:

a sixth NMOS transistor having a source coupled to the ground and a drain coupled to the gate of the third NMOS transistor;

a seventh PMOS transistor having a source coupled to the system voltage and a drain coupled to the drain of the sixth NMOS transistor; and

a seventh NMOS transistor having a gate coupled to the system voltage, a drain coupled to the I/O pad, and a source coupled to gates of the sixth NMOS transistor and the seventh PMOS transistor.